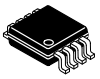
ASM705, ASM706, ASM707, ASM708, ASM813L

Low Power μP Supervisor Circuits

ON Semiconductor®

http://onsemi.com

PDIP−8
P SUFFIX
CASE 646AA



MICRO−8
U SUFFIX
CASE 846AA

SOIC−8
S SUFFIX
CASE 751BD

Description

The ASM705 / 706 / 707 / 708 and ASM813L are cost effective CMOS supervisor circuits that monitor power−supply and battery voltage level, and μP/μC operation.

The family offers several functional options. Each device generates a reset signal during power−up, power−down and during brownout conditions. A reset is generated when the supply drops below 4.65 V (ASM705/707/813L) or 4.40 V (ASM706/708). For 3 V power supply applications, refer to the ASM705P/R/S/T data sheet. In addition, the ASM705/706/813L feature a 1.6 second watchdog timer. The ASM707/708 have both active−HIGH and active−LOW reset outputs but no watchdog function. The ASM813L has the same pin−out and functions as the ASM705 but has an active−HIGH reset output. A versatile power−fail circuit has a 1.25 V threshold, useful in low battery detection and for monitoring non−5 V supplies. All devices have a manual reset ($\overline{MR}$) input. The watchdog timer output will trigger a reset if connected to $\overline{MR}$.

All devices are available in 8−pin DIP, SO and MicroSO packages.

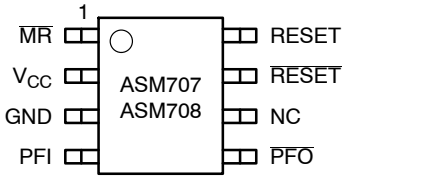
Features

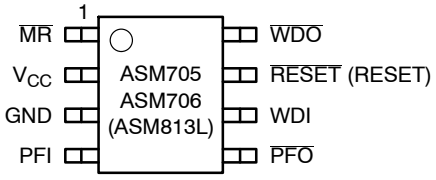
- Precision Power Supply Monitor
  - 4.65 V Threshold (ASM705/707/813L)
  - 4.40 V Threshold (ASM706/708)
- Debounced Manual Reset Input
- Voltage Monitor
  - 1.25 V Threshold
  - Battery Monitor / Auxiliary Supply Monitor
- Watchdog Timer (ASM705/706/813L)
- 200 ms Reset Pulse Width
- Active HIGH Reset Output (ASM707/708/813L)
- MicroSO Package

Applications

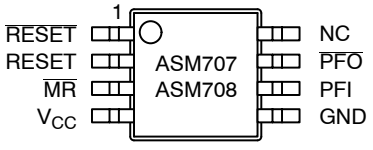
- Computers and Embedded Controllers
- Portable/Battery−operated Systems
- Intelligent Instruments
- Wireless Communication Systems
- PDAs and Hand−held Equipment
- Automotive Systems
- Safety Systems

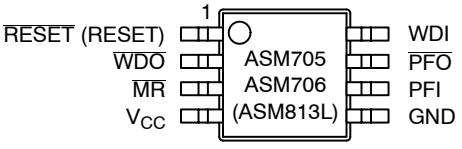
PIN CONFIGURATIONS





DIP/SO
(Top Views)





MicroSO
(Top Views)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

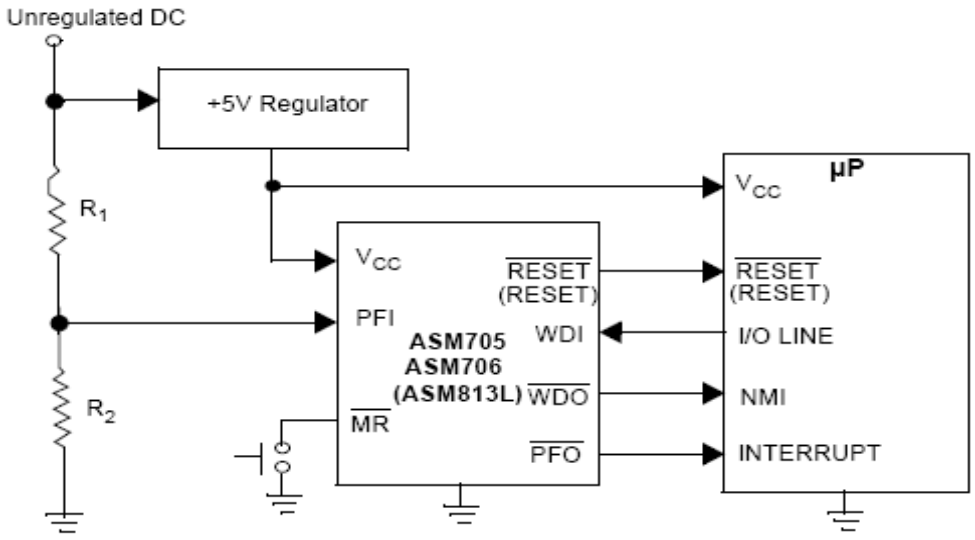


Figure 1. Typical Operating Circuit

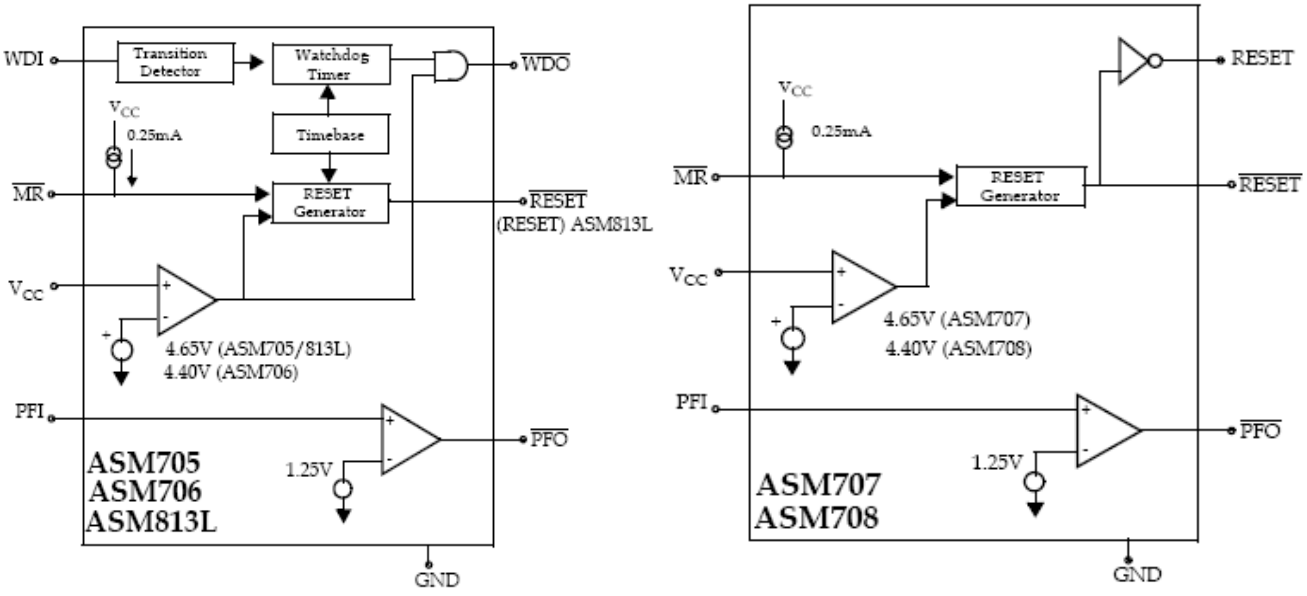


Figure 2. Block Diagrams

Table 1. PIN DESCRIPTION

Pin Number							
ASM705/706		ASM707/708		ASM813L			
DIP/ SO	MicroSO	DIP/ SO	MicroSO	DIP/ SO	MicroSO	Name	Function
1	3	1	3	1	3	$\overline{MR}$	Manual reset input. The active LOW input triggers a reset pulse. A 250 μA pull−up current allows the pin to be driven by TTL/CMOS logic or shorted to ground with a switch.
2	4	2	4	2	4	V_{CC}	+5 V power supply input.
3	5	3	5	3	5	GND	Ground reference for all signals.
4	6	4	6	4	6	PFI	Power−fail input voltage monitor. With PFI less than 1.25 V, $\overline{PFO}$ goes LOW. Connect PFI to Ground or V_{CC} when not in use.
5	7	5	7	5	7	$\overline{PFO}$	Power−fail output. The output is active LOW and sinks current when PFI is less than 1.25 V.
6	8	−	−	6	8	WDI	Watchdog input. WDI controls the internal watchdog timer. A HIGH or LOW signal for 1.6 sec at WDI allows the internal timer to run−out, setting $\overline{WDO}$ LOW. The watchdog function is disabled by floating WDI or by connecting WDI to a high impedance three−state buffer. The internal watchdog timer clears when: RESET is asserted; WDI is three−stated; or WDI sees a rising or falling edge.
−	−	6	8	−	−	NC	Not Connected.
7	1	7	1	−	−	$\overline{RESET}$	Active LOW reset output. Pulses LOW for 200 ms when triggered, and stays LOW whenever V_{CC} is below the reset threshold. $\overline{RESET}$ remains LOW for 200 ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from LOW to HIGH. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	2	−	−	8	2	$\overline{WDO}$	Watchdog output. $\overline{WDO}$ goes LOW when the 1.6 second internal watchdog timer times−out and does not go HIGH until the watchdog is cleared. In addition, when V_{CC} falls below the reset threshold, $\overline{WDO}$ goes LOW. Unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width and as soon as V_{CC} exceeds the reset threshold, $\overline{WDO}$ goes HIGH with no delay.
−	−	8	2	7	1	RESET	Active HIGH reset output. The inverse of RESET. The ASM813L only has a $\overline{RESET}$ output.

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
Pin Terminal Voltage with Respect to Ground V_{CC} All other inputs (Note 1) Input Current at V_{CC} and GND	 −0.3 −0.3	 6.0 V_{CC} + 0.3 20	 V V mA
Output Current: All outputs		20	mA
Rate of Rise at V_{CC}		100	V/μs
Plastic DIP Power Dissipation (Derate 9 mW/°C above 70°C)		700	mV
SO Power Dissipation (Derate 5.9 mW/°C above 70°C)		470	mW
MicroSO Power Dissipation (Derate 4.1 mW/°C above 70°C)		330	mW
Operating Temperature Range ASM705E/706E/707E/708E/813LE ASM705C/706C/707C/708C/813LC	 −40 0	 +85 70	°C
Storage Temperature Range	−65	160	°C
Lead Temperature (Soldering 10 sec)		300	°C
ESD rating HBM MM		 2 200	 KV V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The input voltage limits of PFI and $\overline{MR}$ can be exceeded if the input current is less than 10 mA.

Table 3. ELECTRICAL CHARACTERISTICS
Unless otherwise noted, specifications are over the operating temperature range and V_{CC} supply voltages are 2.7 V to 5.5 V (ASM706P,ASM708R), 3.0 V to 5.5 V (ASM706/708S), 3.15 V to 5.5 V (ASM706/708T) and 4.1 V to 5.5 V (ASM706/708J).

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating Voltage Range	V_{CC}	ASM705/6/7/8C	1.2		5.5	V
		ASM813L	1.1		5.5	
		ASM705/6/7/8E, ASM813E	1.2		5.5	
Supply Current	I_{CC}	ASM705/706C/813LC		75	140	μA
		ASM705E/706E/813LE		75	140	
		ASM707C/708C		50	140	
		ASM707E/708E		50	140	
RESET Threshold	V_{RT}	ASM705/707/813L (Note 2)	4.50	4.65	4.75	V
		ASM706/708 (Note 2)	4.25	4.40	4.50	
RESET Threshold Hysteresis		(Note 2)		40		mV
RESET Pulse Width	t_{RS}	(Note 2)	140	200	280	ms
$\overline{MR}$ Pulse Width	t_{MR}		0.15			μs
$\overline{MR}$ to RESET Out Delay	t_{MD}	(Note 2)			0.25	μs
$\overline{MR}$ Input Threshold	V_{IH}		2.0			V
	V_{IL}				0.8	
$\overline{MR}$ Pullup current		MR = 0 V	100	250	600	μA
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800 μA	V_{CC} – 1.5			V
		I_{SINK} = 3.2 mA			0.4	
		ASM705/6/7/8, V_{CC} = 1.2 V, I_{SINK} = 100 μA			0.3	
RESET Output Voltage		ASM707/8/813L, I_{SOURCE} = 800 μA	V_{CC} – 1.5			V
		ASM707/8, I_{SINK} = 1.2 mA			0.4	
		ASM813L, I_{SINK} = 3.2 mA			0.4	
		ASM813L, V_{CC} = 1.2 V, I_{SOURCE} = 4 μA	0.9			
Watchdog Timeout Period	t_{WD}	ASM705/6/813L	1.00	1.60	2.25	S
WDI Pulse Width	t_{WP}	V_{IL} = 0.4 V, V_{IH} = 0.8 V_{CC}	50			ns
WDI Input Threshold	V_{IH}	ASM705/706/813L, V_{CC} = 5 V	3.5			V
	V_{IL}				0.8	
WDI Input Current		ASM705/6/813L, WDI = V_{CC}		50	150	μA
		ASM705/6/813L, WDI = 0 V	–150	–50		
$\overline{WDO}$ Output Voltage	V_{OH}	ASM705/6/813L, I_{SOURCE} = 800 μA	V_{CC} – 1.5			V
	V_{OL}	ASM705/6/813L, I_{SINK} = 1.2 mA			0.4	
PFI Input Threshold		V_{CC} = 5 V	1.2	1.25	1.3	V
PFI Input Current			–25	0.01	25	nA
$\overline{PFO}$ Output Voltage	V_{OH}	I_{SOURCE} = 800 μA	V_{CC} – 1.5			V
	V_{OL}	I_{SINK} = 3.2 mA			0.4	

2. $\overline{RESET}$ (ASM705/6/7/8), RESET(ASM707/8, ASM813L)

Detailed Description

A proper reset input enables a microprocessor / microcontroller to start in a known state. ASM70X and ASM813L assert reset to prevent code execution errors during power−up, power−down and brown−out conditions.

RESET/$\overline{\text{RESET}}$ Timing

The RESET/$\overline{\text{RESET}}$ signals are designed to start a μP/μC in a known state or return the system to a known state.

The ASM707/708 have two reset outputs, one active−HIGH RESET and one active−LOW $\overline{\text{RESET}}$ output. The ASM813L has only an active−HIGH output. $\overline{\text{RESET}}$ is simply the complement of RESET.

$\overline{\text{RESET}}$ is guaranteed to be LOW with V_{CC} above 1.2 V.

During a power−up sequence, $\overline{\text{RESET}}$ remains low until the supply rises above the threshold level, either 4.65 V or 4.40 V. $\overline{\text{RESET}}$ goes high approximately 200 ms after crossing the threshold.

During power−down, $\overline{\text{RESET}}$ goes LOW as V_{CC} falls below the threshold level and is guaranteed to be under 0.4 V with V_{CC} above 1.2 V.

In a brownout situation where V_{CC} falls below the threshold level, $\overline{\text{RESET}}$ pulses low. If a brown−out occurs during an already initiated reset, the pulse will continue for a minimum of 140 ms.

Power Failure Detection with Auxiliary Comparator

All devices have an auxiliary comparator with 1.25 V trip point and uncommitted output ($\overline{\text{PFO}}$) and noninverting input (PFI). This comparator can be used as a supply voltage monitor with an external resistor voltage divider. The attenuated voltage at PFI should be set just below the 1.25 threshold. As the supply level falls, PFI is reduced causing the $\overline{\text{PFO}}$ output to transit LOW. Normally $\overline{\text{PFO}}$ interrupts the processor so the system can be shut down in a controlled manner.

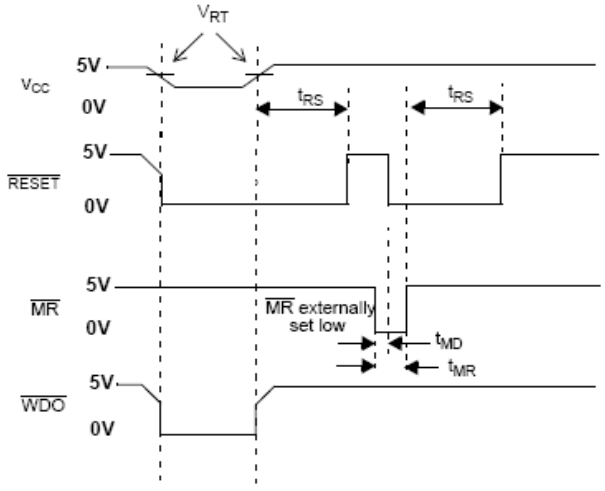


Figure 3. WDI Three−state Operation

Manual Reset ($\overline{\text{MR}}$)

The active−LOW manual reset input is pulled high by a 250 μA pull−up current and can be driven low by CMOS/TTL logic or a mechanical switch to ground. An external debounce circuit is unnecessary since the 140 ms minimum reset time will debounce mechanical pushbutton switches.

By connecting the watchdog output ($\overline{\text{WDO}}$) and $\overline{\text{MR}}$, a watchdog timeout forces $\overline{\text{RESET}}$ to be generated. The ASM813L should be used when an active−HIGH RESET is required.

Watchdog Timer

The watchdog timer available on the ASM705/706/813L monitors μP/μC activity. An output line on the processor is used to toggle the WDI line. If this line is not toggled within 1.6 seconds, the internal timer puts the watchdog output, $\overline{\text{WDO}}$, into a LOW state. $\overline{\text{WDO}}$ will remain LOW until a toggle is detected at WDI.

If WDI is floated or connected to a three−stated circuit, the watchdog function is disabled, meaning, it is cleared and not counting. The watchdog timer is also disabled if RESET is asserted. When RESET becomes inactive and the WDI input sees a high or low transition as short as 50 ns, the watchdog timer will begin a 1.6 second countdown. Additional transitions at WDI will reset the watchdog timer and initiate a new countdown sequence.

$\overline{\text{WDO}}$ will also become LOW and remain so, whenever the supply voltage, V_{CC}, falls below the device threshold level. $\overline{\text{WDO}}$ goes HIGH as soon as V_{CC} transitions above the threshold. There is no minimum pulse width for $\overline{\text{WDO}}$ as there is for the RESET outputs. If WDI is floated, $\overline{\text{WDO}}$ essentially acts as a low−power output indicator.

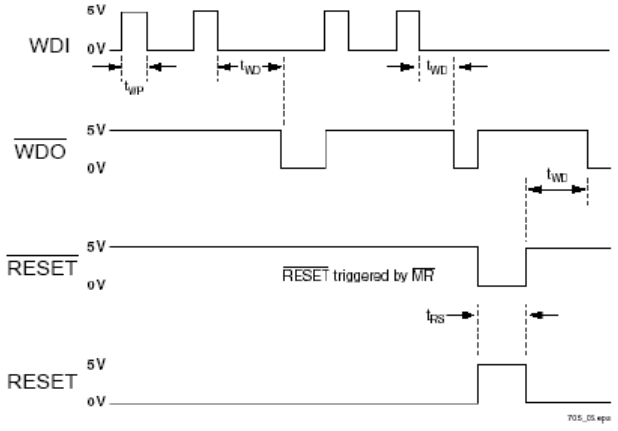


Figure 4. Watchdog Timing

Application Information

Ensuring That $\overline{\text{RESET}}$ is Valid Down to V_{CC} = 0 V

When V_{CC} falls below 1.1 V, the ASM705−708 $\overline{\text{RESET}}$ output no longer pulls down; it becomes indeterminate. To avoid the possibility that stray charges build up and force $\overline{\text{RESET}}$ to the wrong state, a pull−down resistor should be connected to the $\overline{\text{RESET}}$ pin, thus draining such charges to ground and holding $\overline{\text{RESET}}$ low. The resistor value is not critical. A 100 kΩ resistor will pull $\overline{\text{RESET}}$ to ground without loading it.

Bi−directional Reset Pin Interfacing

The ASM705/6/7/8 can interface with µP/µC bi−directional reset pins by connecting a 4.7 kΩ resistor in series with the $\overline{\text{RESET}}$ output and the µP/µC bi−directional $\overline{\text{RESET}}$ pin.

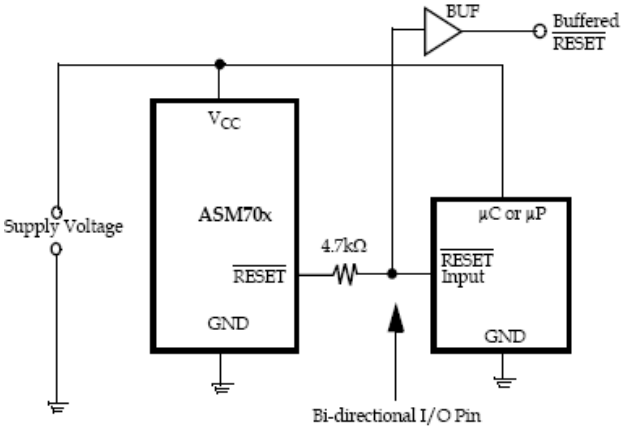


Figure 5. Bi−directional Reset Pin Interfacing

Monitoring Voltages Other Than VCC

The ASM705−708 can monitor voltages other than V_{CC} using the Power Fail circuitry. If a resistive divider is connected from the voltage to be monitored to the Power Fail input (PFI), the $\overline{\text{PFO}}$ will go LOW if the voltage at PFI goes below 1.25 V reference. Should hysteresis be desired, connect a resistor (equal to approximately 10 times the sum of the two resistors in the divider) between the PFI and $\overline{\text{PFO}}$ pins. A capacitor between PFI and GND will reduce circuit sensitivity to input high−frequency noise. If it is desired to assert a $\overline{\text{RESET}}$ for voltages other than V_{CC} then the $\overline{\text{PFO}}$ output is to be connected to the $\overline{\text{MR}}$.

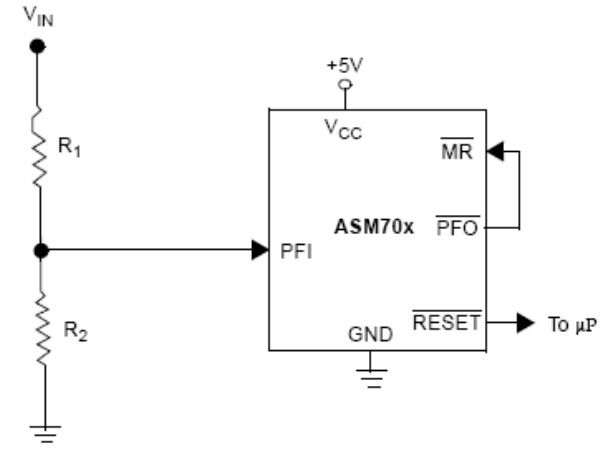


Figure 6. Monitoring +5 V and an Additional Supply V_{IN}

Monitoring a Negative Voltage

The Power−Fail circuitry can also monitor a negative supply rail. When the negative rail is OK, $\overline{\text{PFO}}$ will be LOW, and when the negative rail is failing (not negative enough), $\overline{\text{PFO}}$ goes HIGH (the opposite of when positive voltages are monitored). To trigger a reset, these outputs need to be inverted: adding the resistors and transistor as shown achieves this. The $\overline{\text{RESET}}$ output will then have the same sense as for positive voltages: good = HIGH, bad = LOW. It should be noted that this circuit's accuracy depends on the V_{CC} line, the PFI threshold tolerance, and the resistors.

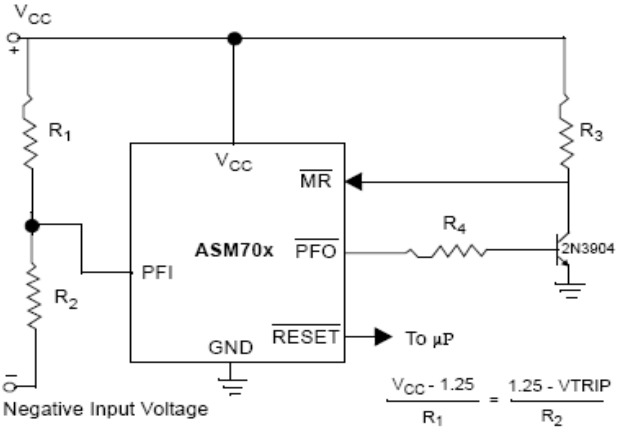
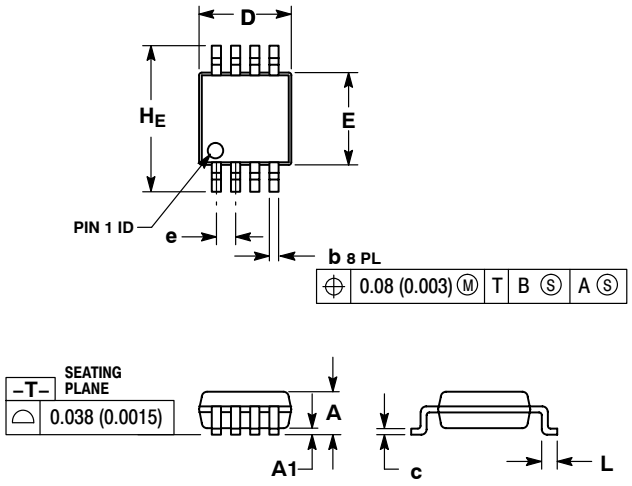


Figure 7. Monitoring a Negative Voltage

PACKAGE DIMENSIONS

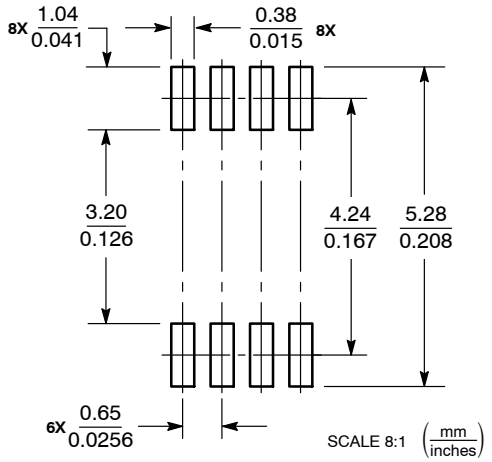
Micro8™/TSSOP8 3x3
CASE 846AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	−−	−−	1.10	−−	−−	0.043
A1	0.05	0.08	0.15	0.002	0.003	0.006
b	0.25	0.33	0.40	0.010	0.013	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
e	0.65 BSC			0.026 BSC		
L	0.40	0.55	0.70	0.016	0.021	0.028
H_E	4.75	4.90	5.05	0.187	0.193	0.199

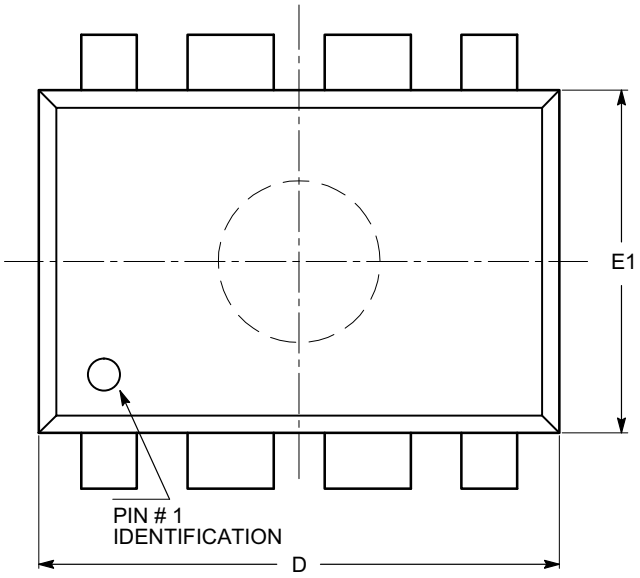
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

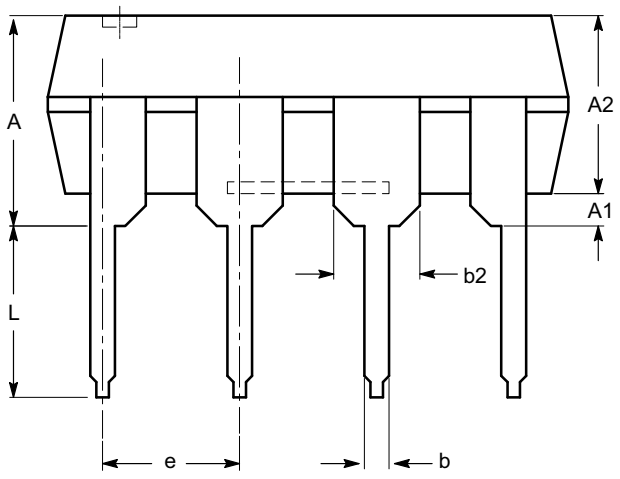
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

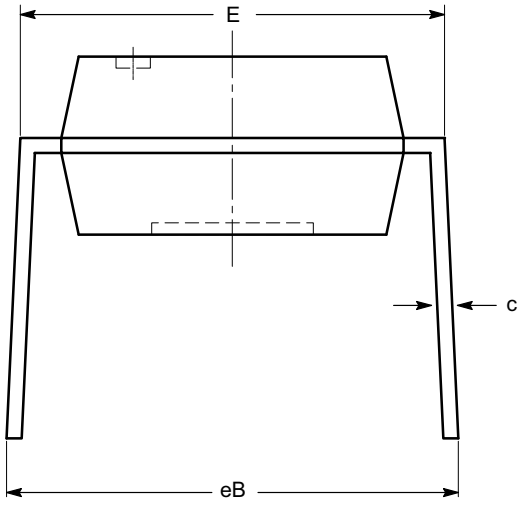


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

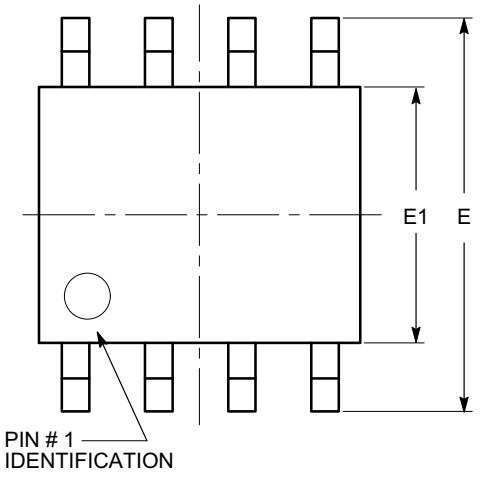


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

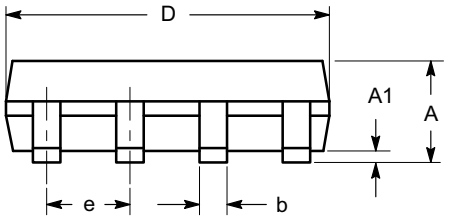
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

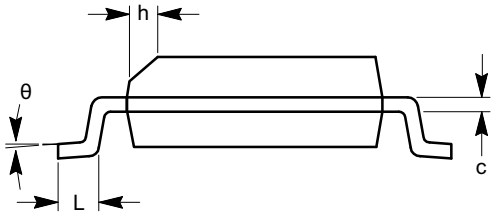


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

Table 4. ORDERING INFORMATION – Tin – Lead Devices

Part Number (Note 3)	**Reset Threshold (V)**	**Temperature (°C)**	**Pins–Package**	**Package Marking**
ASM705 Active LOW Reset, Watchdog Output And Manual RESET				
ASM705CPA	4.65	0°C to +70°C	8–Plastic DIP	ASM705CPA
ASM705CSA	4.65	0°C to +70°C	8–SO	ASM705CSA
ASM705CUA	4.65	0°C to +70°C	8–MicroSO	ASM705CUA
ASM705EPA	4.65	–40°C to +85°C	8–Plastic DIP	ASM705EPA
ASM705ESA	4.65	–40°C to +85°C	8–SO	ASM705ESA
ASM705EUA	4.65	–40°C to +85°C	8–MicroSO	ASM705EUA
ASM706 Active LOW Reset, Watchdog Output And Manual RESET				
ASM706CPA	4.40	0°C to +70°C	8–Plastic DIP	ASM706CPA
ASM706CSA	4.40	0°C to +70°C	8–SO	ASM706CSA
ASM706CUA	4.40	0°C to +70°C	8–MicroSO	ASM706CUA
ASM706EPA	4.40	–40°C to +85°C	8–Plastic DIP	ASM706EPA
ASM706ESA	4.40	–40°C to +85°C	8–SO	ASM706ESA
ASM707 Active LOW & HIGH Reset with Manual RESET				
ASM707CPA	4.65	0°C to +70°C	8–Plastic DIP	ASM707CPA
ASM707CSA	4.65	0°C to +70°C	8–SO	ASM707CSA
ASM707CUA	4.65	0°C to +70°C	8–MicroSO	ASM707CUA
ASM707EPA	4.65	–40°C to +85°C	8–Plastic DIP	ASM707EPA
ASM707ESA	4.65	–40°C to +85°C	8–SO	ASM707ESA
ASM708Active LOW & HIGH Reset with Manual RESET				
ASM708CPA	4.40	0°C to +70°C	8–Plastic DIP	ASM708CPA
ASM708CSA	4.40	0°C to +70°C	8–SO	ASM708CSA
ASM708CUA	4.40	0°C to +70°C	8–MicroSO	ASM708CUA
ASM708EPA	4.40	–40°C to +85°C	8–Plastic DIP	ASM708EPA
ASM708ESA	4.40	–40°C to +85°C	8–SO	ASM708ESA
ASM813L Active HIGH Reset, Watchdog Output And Manual RESET				
ASM813LCPA	4.65	0°C to +70°C	8–Plastic DIP	ASM813LCPA
ASM813LCSA	4.65	0°C to +70°C	8–SO	ASM813LCSA
ASM813LCUA	4.65	0°C to +70°C	8–MicroSO	ASM813LCUA
ASM813LEPA	4.65	–40°C to +85°C	8–Plastic DIP	ASM813LEPA
ASM813LESA	4.65	–40°C to +85°C	8–SO	ASM813LESA

3. For parts to be packed in Tape and Reel, add “–T” at the end of the part number.

Table 5. ORDERING INFORMATION – Lead Free Devices

Part Number (Note 4)	**Reset Threshold (V)**	**Temperature (°C)**	**Pins–Package**	**Package Marking**
ASM705 Active LOW Reset, Watchdog Output And Manual RESET				
ASM705CPAF	4.65	0°C to +70°C	8–Plastic DIP	ASM705CPAF
ASM705CSAF	4.65	0°C to +70°C	8–SO	ASM705CSAF
ASM705CUAF	4.65	0°C to +70°C	8–MicroSO	ASM705CUAF
ASM705EPAF	4.65	–40°C to +85°C	8–Plastic DIP	ASM705EPAF
ASM705ESAF	4.65	–40°C to +85°C	8–SO	ASM705ESAF
ASM705EUAF	4.65	–40°C to +85°C	8–MicroSO	ASM705EUAF
ASM706 Active LOW Reset, Watchdog Output And Manual RESET				
ASM706CPAF	4.40	0°C to +70°C	8–Plastic DIP	ASM706CPAF
ASM706CSAF	4.40	0°C to +70°C	8–SO	ASM706CSAF
ASM706CUAF	4.40	0°C to +70°C	8–MicroSO	ASM706CUAF
ASM706EPAF	4.40	–40°C to +85°C	8–Plastic DIP	ASM706EPAF
ASM706ESAF	4.40	–40°C to +85°C	8–SO	ASM706ESAF
ASM707 Active LOW & HIGH Reset with Manual RESET				
ASM707CPAF	4.65	0°C to +70°C	8–Plastic DIP	ASM707CPAF
ASM707CSAF	4.65	0°C to +70°C	8–SO	ASM707CSAF
ASM707CUAF	4.65	0°C to +70°C	8–MicroSO	ASM707CUAF
ASM707EPAF	4.65	–40°C to +85°C	8–Plastic DIP	ASM707EPAF
ASM707ESAF	4.65	–40°C to +85°C	8–SO	ASM707ESAF
ASM708Active LOW & HIGH Reset with Manual RESET				
ASM708CPAF	4.40	0°C to +70°C	8–Plastic DIP	ASM708CPAF
ASM708CSAF	4.40	0°C to +70°C	8–SO	ASM708CSAF
ASM708CUAF	4.40	0°C to +70°C	8–MicroSO	ASM708CUAF
ASM708EPAF	4.40	–40°C to +85°C	8–Plastic DIP	ASM708EPAF
ASM708ESAF	4.40	–40°C to +85°C	8–SO	ASM708ESAF
ASM813L Active HIGH Reset, Watchdog Output And Manual RESET				
ASM813LCPAF	4.65	0°C to +70°C	8–Plastic DIP	ASM813LCPAF
ASM813LCSAF	4.65	0°C to +70°C	8–SO	ASM813LCSAF
ASM813LCUAF	4.65	0°C to +70°C	8–MicroSO	ASM813LCUAF
ASM813LEPAF	4.65	–40°C to +85°C	8–Plastic DIP	ASM813LEPAF
ASM813LESAF	4.65	–40°C to +85°C	8–SO	ASM813LESAF

4. For parts to be packed in Tape and Reel, add “–T” at the end of the part number.

Table 6. FEATURE SUMMARY

	ASM705	ASM706	ASM707	ASM708	ASM813L
Power fail detector	♦	♦	♦	♦	♦
Brownout detection	♦	♦	♦	♦	♦
Manual RESET input	♦	♦	♦	♦	♦
Power−up/down RESET	♦	♦	♦	♦	♦
Watchdog Timer	♦	♦			♦
Active HIGH RESET output			♦	♦	♦
Active LOW RESET output	♦	♦	♦	♦	
RESET Threshold (V)	4.65	4.40	4.65	4.40	4.65

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